A FREQUENCY TRANSLATOR USING DUAL-GATE GaAs FETs

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ABSTRACT

An active 11.5 GHz frequency translator using four dual-gate FETs has been developed. Carrier and spurious sideband suppression of more than 20 dB has been achieved for translation frequency of up to 1 MHz. The same circuit can also be used as a high speed QPSK modulator with phase transition time of about 1 nanosecond.

INTRODUCTION

A frequency translator is often used to generate a false target signal to deceive a hostile radar. Basically, there are three types of frequency translators that are often considered, namely: (i) A Serrodyne frequency translator consisting of a pair of balanced mixers located in quadrature and driven by a pair of quadrature modulation signals. (ii) A chain of digital phase shifters to obtain a staircase 360° phase shift [1-3] and (iii) A continuous 360° phase shift using analog phase shifter.[10]

Due to the frequency mixing process in the first type of frequency translator, the carrier and unwanted sideband suppression of more than 15 dB is generally very difficult to obtain.

In the second type of frequency translator using a chain of digital phase shifters, the spurious suppression depends on the number of phase shift bits and also on the accuracy of the phase shift in each bit. A 20 dB spurious suppression generally requires a 4-bit (16 steps) digital phase shifter. It requires a complex driver circuit design and also the translation frequency is often limited by the phase switching speed of each bit.

In the third type of frequency translator, the 360° analog phase shifting is generally realized using varactor diodes. Since the junction capacitance of the varactor diode is a non-linear function of the drive voltage, a constant rate of phase shift over the entire 360° cycle, which is the condition for a spurious free frequency translation, is also very difficult to achieve.

High speed active digital phase shifter and continuously variable phase shifter utilizing dual-gate FETs have been reported recently. [4-9] In this paper we will describe a FET continuous phase shifter developed for frequency translation application.

The active frequency translator to be described here consists of four dual-gate FET amplifiers located in four parallel paths which are off-set sequentially by 90° incremental phase shift. The control gates of the FETs are driven by appropriate analog signals which are generated based on sinusoidal waveforms. More than 20 dB suppression of unwanted spurious levels has been achieved for translation frequencies up to 1 MHz.

The same circuit can also be used as a high-speed QPSK modulator with phase transition time of about 1 nanosecond.

CIRCUIT DESCRIPTION AND PRINCIPLE OF OPERATION

Figure 1(a) shows the schematic of the frequency translator. The input signal is divided into four equal amplitude signals which are then sequentially off-set by 90° incremental phase shift. Each signal is amplified by a dual-gate FET amplifier whose gain can be controlled by the second gate control voltage. The outputs of the four paths are then combined.

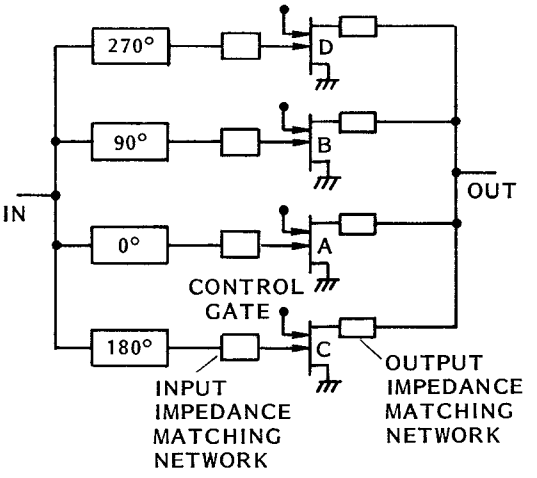

Fig. 1(a). Schematic of the Frequency Translator Using Four Dual-Gate FETs.

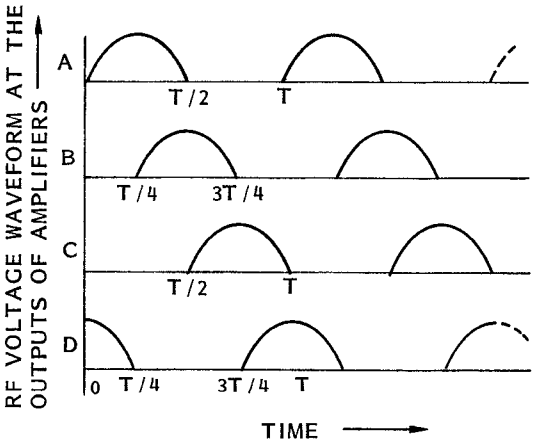

Fig. 1(b). Timing Diagram for Ideal Frequency Translator Operation Showing Variation of the Output RF Voltage Waveform in Each Amplifier Path.

For an ideal spurious-free frequency translator operation, the driving waveforms at the control gates of the dual-gate FETs are to be so designed as to obtain half sinusoidal variation in the rf output voltage at each path and sequenced as shown in Figure 1(b). At any instant only two amplifier paths provide rf signals. For example, during o-T/4, amplifiers A and D provide outputs which are

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combined in quadrature. Thus, if the outputs of A and D are varied sinusoidally then the output of the combined signal has constant amplitude and constant rate of phase shift from -90° to 0°. Similarly, during T/4 to T/2, the amplifiers A and B provide the outputs in quadrature which are combinded to result in constant amplitude and constant rate of phase shift from 0° to 90°. In the same manner, the continuous phase variation from 90° to 180° and from 180° to -90° are provided during T/2 to 3T/4 and 3T/4 to T , respectively. Thus the 360° phase shift is achieved in time T, the period of the translation frequency.

Any deviation from (i) sinusidal variation of the rf output voltage waveform of each amplifier path, (ii) the 90° phase off-set of each path and (iii) the amplitude balance in the amplifier paths, will result in amplitude ripple and non-constant rate of phase shift. Both amplitude ripple and non-constant rate of pahse shift will generate the unwanted spurious sidebands in addition to the translated frequency.

CIRCUIT REALIZATION AND EXPERIMENTAL PERFORMANCE

The frequency translator, using four Raytheon RDX41 dual-gate GaAs FETs, has been realized on alumina substrate. The four-way divider/combiner circuits used in the translator are realized by cascading Wilkinson split-tee dividers. The phase off-sets in the four paths are realized by lengths of transmission line. The circuit is made symmetrical by equally distributing the phase off-sets on both sides of the FET amplifier in each path. A photograph of the frequency translator is shown in Figure 2.

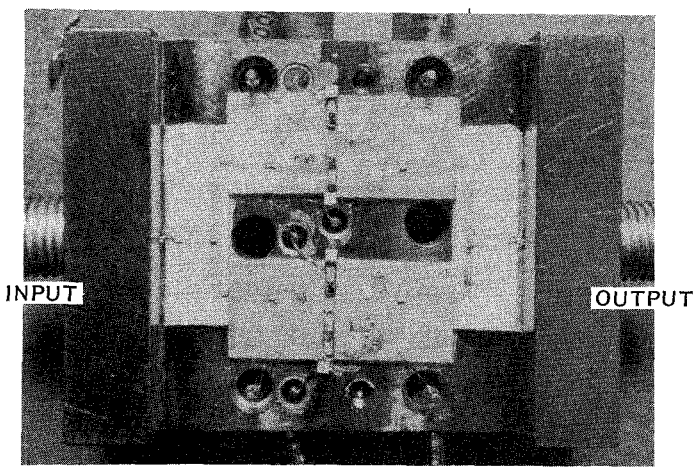

Fig. 2. Photograph of the Frequency Translator Circuit.

The dual-gate FETs were characterized by measured S-parameters for first gate bias V_{G1S} = -1V, second gate bias V_{G2S} = 0V and drain voltage V_{DS} = 7 V. The matching networks for the amplifiers were then designed and optimized using COMPACT for a typical gain of 8 dB over 10% bandwidth centered at 11.5 GHz.

The design of the frequency translator was verified by static measurements. This involves measuring the gain of each amplifier (when V_{G1S} = -1V, V_{G2S} = 0V) while the other three are turned "OFF" (V_{G1S} = -1V, V_{G2S} = -5V). It was found that the four amplifier path gains were balanced within $\pm$ 1 dB over 10% bandwidth and within $\pm$ 0.5 dB over 5% bandwidth centered at 11.5 GHz. Each amplifier had an isolation from "ON" (V_{G2S} = 0) to "OFF" ($V_{G2S} \leq$ -3V) of more than 25 dB.

To realize the output rf voltage waveforms, shown in Figure 1(b), at the amplifier paths, a driver circuit was designed. The driver circuit, driven by a sinewave signal at the translation frequency, produces four outputs to be applied to the four control gates of the dual-gate FETs. By adjusting the amplitude of the input sinewave signal, the four output signals of the driver circuit can be distorted to the extent required for making the output rf voltage waveforms at each amplifier path closely approximate to those of Figure 1(b). The four control signals are found to be approximately sinusoidal with DC offset, varying from 0 to -6V, as shown in Figure 3(a). When the control gates of the four FETs are driven by the waveforms shown in Figure 3(a), the output spectrum of the frequency translator was measured as showed in Figure 3(b). It is seen that the unwanted spurious levels, i.e. the carrier and undesired sidebands, are suppressed more than 20 dB with respect to the translated frequency signal.

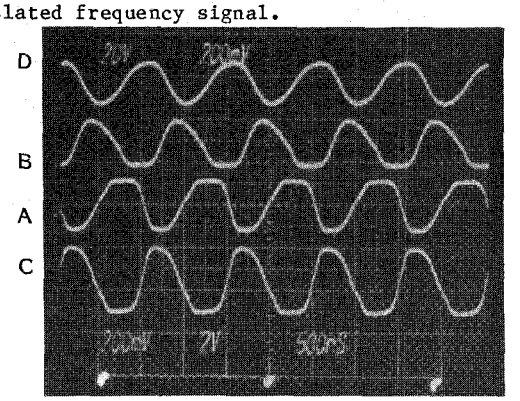

Fig. 3(a). Analog Driving Waveforms at the Control Gates of the Four FETs. Frequency 1 MHz.

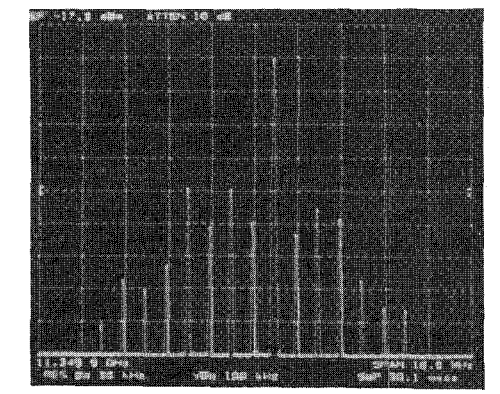

Fig. 3(b). Output Spectrum of the Frequency Translator when the Control Gates of the FETs are Driven by the Waveforms Shown in Figure 3(a). Vert: 5 dB/div.

In some applications, where the spurious sideband suppression of about 10 dB can be tolerated, the same translator circuit can be operated as a 2-bit (4-step QPSK) digital phase shifter. For this purpose the control gates of the four FETs are driven by properly sequenced square wave signals which can be realized by simple driver circuits. Figure 4(b) shows the output spectrum of the frequency translator when used as a 2-bit digital phase shifter by driving the control gates of the FETs with the square waveforms as shown in Figure 4(a). In the digital phase shifter mode the phase switching time was measured to be about 1 nanosecond which is mainly limited by the driver circuits used.

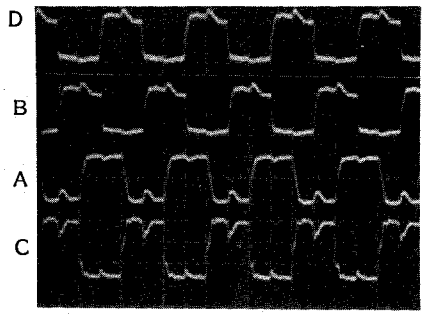

Fig. 4(a). Digital Driving Waveforms at the Control Gates of the FETs for 2-Bit Phase Shifter Operation. Frequency 1 MHz.

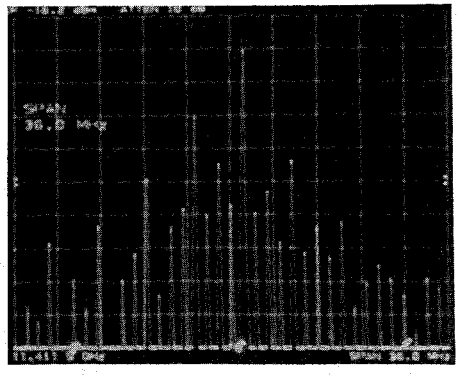

Fig. 4(b). Output Spectrum of the Frequency Translator When the Control Gates of the FETs are Driven by the Waveforms Shown in Figure 4(a). Vert: 5 dB/div.

CONCLUSIONS

A frequency translator at 11.5 GHz using four dual-gate GaAs FETs is described. The performances of the translator when used as a 2-bit 4-step digital phase shifter and as a 360° continuous phase shifter are presented. It has been found that the unwanted spurious levels at the output of the translator are suppressed by more than 20 dB when the control gates of the FETs are driven by properly sequenced approximately sinusoidal waveforms.

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